Design and Analysis of Two-Stage Amplifier

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Design and Analysis of Two-Stage Amplifier

Introduction

This report discusses the design and analysis of a two stage amplifier. An FET based common source amplifier was designed.FET was preferred over BJT because of the following reasons [1] [4]

- FETs are voltage operated devices, so consumes less power.
- FETs have high input impedance

Common source amplifier was preferred over Common gate or common drain because of its high gain, high bandwidth and high input impedance.[1]

Specifications of the Amplifier

Number of stages: 2
Bandwidth: 10 KHz
Gain: 2.8

Circuit Diagram

Two identical single stage amplifiers are combined to get a two-stage amplifier.

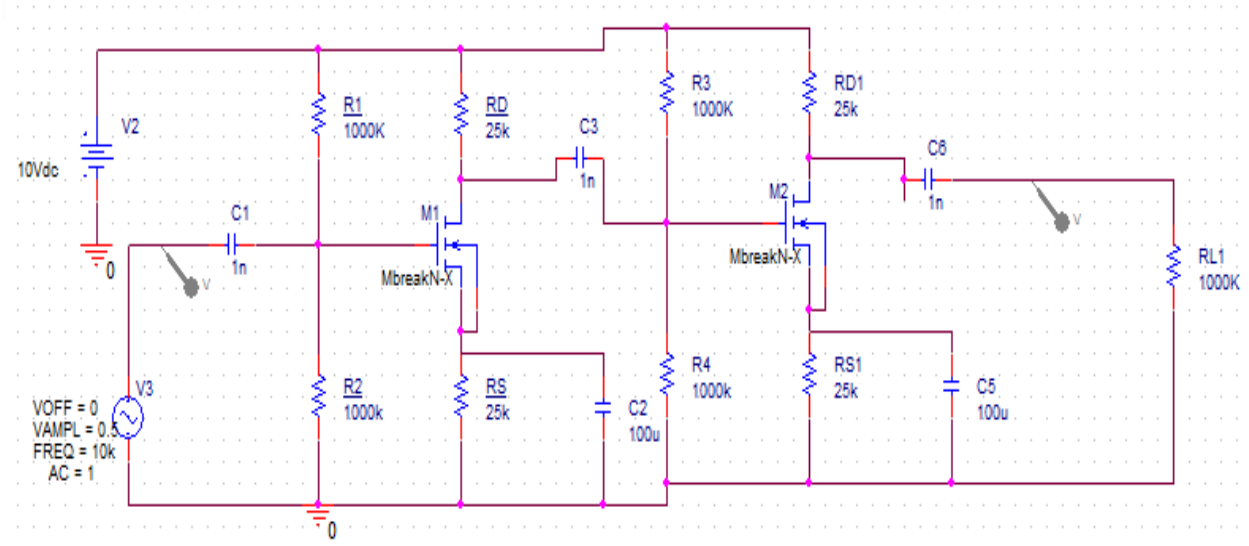

Figure 1 Circuit Diagram

Fig: 1 shows the circuit diagram of the common source two stage amplifier.

R1 and R2 are used for biasing the MOSFET. They determine the input impedance of the amplifier. They must be high to have a high gain.C1 is the input decupling capacitor, which is used to remove the DC component of the signal to be amplified. Its value must be high to have a high gain at lower signal frequency. It determines low frequency gain of the amplifier. R_D determines the gain of the amplifier. For higher gain R_D must be

high.C2 is called bypass capacitor, used to bypass the signal to ground. When C2 is removed, signal will get dropped across R_S and it gives a negative feedback. So gain reduces. If C2 is not present and neglecting the effect of C1 gain will be gm R1/(1+ gmR2) [2]

DC Analysis

For DC analysis all the capacitors are neglected (considered as open circuit).

Since both the stages are identical, analysis of only signle stage is presented here.

VDD= 10V

$V_{DS} = V_{DD}/2 = 5V$

Take I_D= 0.1 mA

$I_D = (V_{DD} - V_{DS})/(R_D+R_S) = 5/(R_D+R_S)$

$R_D + R_S = 5/0.1\ mA = 50\ K;$

Take $R_D = R_S = 25K$

Gate Current, $I_G = 0$ mA

Let $R_1 = R_2 = R$

$V_G = V_{DD}/2 = 5V$

Input impedance is determined by R_1 and R_2. In order to avoid loading of the signal source, we need to select a high value of R_1 and R_2.

Take $R_1 = R_2 = 1M$

Biasing Analysis

Voltage divider biasing was used.

Following are the biasing conditions

$V_{DS} = 5V$

$I_D = 0.1mA$

Voltage at gate, $V_G = 5V$

Voltage at source, $V_S = 2.5V$

Voltage at drain, $V_S = 7.5V$

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V_{GS} - V_G- V_S = 5 -2.5 = 2.5V

Load Line analysis

Operating point of the amplifier is found by drawing the DC load line. Operating point or Q-point is the intersection of the DC-load line (circuit characteristics) with device characteristics. For getting maximum swing of the output voltage, we should fix the Q-point at the center of the DC load line. If Q-point is at the center of the load line, Max swing possible = $V_{DD}/2$ in either direction.

Drawing The DC Load Line

$I_D(R_D + R_S) + V_{DS} = V_{DD}$

Graph of the above equation with VDS in x-axis and ID in Y-axis is the load line

When V_{DS} = 0, ID = $V_{DD}/(R_D + R_S)$ = 10/50K = 0.2mA, so (0,0.2) is a point on the graph

When I_D = 0, V_{DS} = V_{DD} = 10V, so (10,0) is appoint on the graph

Joining the above two points bay a straight line will give the DC-load line.

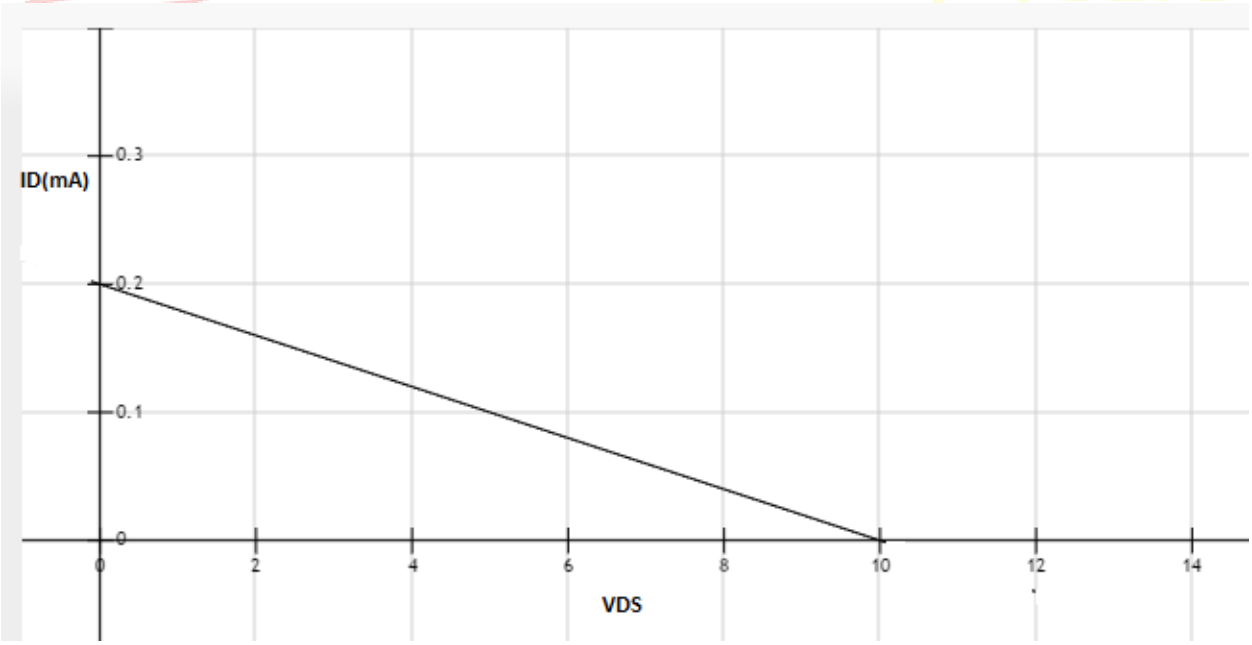

Figure 2 DC-Load Line

Figure: 3 shows the Q-point of the amplifier.

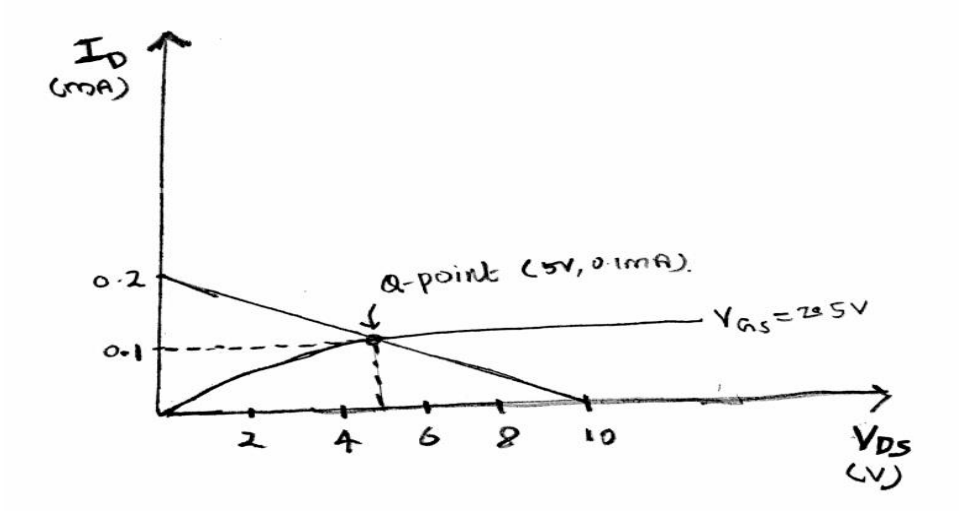

Figure 3 Q-Point

AC Analysis

Theoretical gain Calculation

Without considering the effect of C1(input coupling capacitor)

Av = gm R_D
$V_{GS} = V_G - V_S = 5 - 2.5 = 2.5$ V
Gm is the Transconductance of the MOSFET which is found by the below formula.
gm = Kn' X W/L $(V_{GS} - V_t)$= 9u X 5 X (2.5 -1) = 9u X 5 X 1.5 = 0.0689 mA/V
Av = 0.0689 mA/V X 25 k= 1.72

Considering the effect of C1

$Xc1 = 1/2*pi*f*C1 = 1/(2*3.14*10*1000*1*10^{-9}) = 15.923K$
$R_G = R1||R2 = 500K$
Gain = 1.72 X RG/ (RG+ Xc1) = 1.72 X 500/(500 + 15.923) =1.67
Total gain = Product of two gains = 1.67 x 1.67 = 2.8

Small Signal Equivalent Circuit[5]

For small signal equivalent circuit derivation, all the capacitor is assumed to be short-circuited. MOSFET is replaced by its small signal equivalent model [6]. Source resistance RS is not having any effect in small signal analysis as C_S will bypass it.

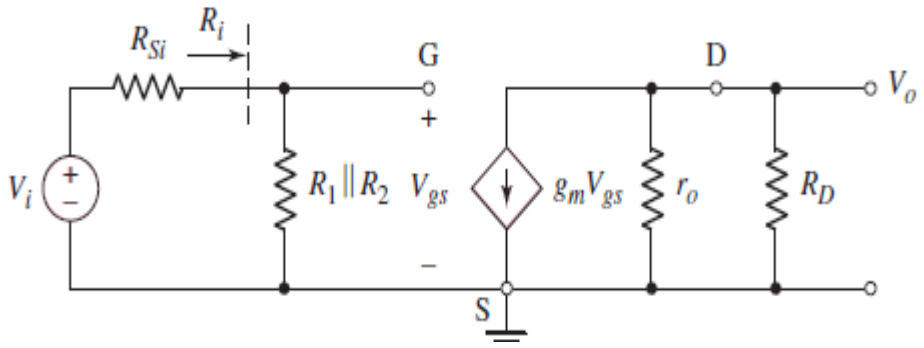

Figure 4 Small Signal Equivalent Circuit

Fig: 3 shows the small signal equivalent circuit of the amplifier.

ro = MOSFET output resistance

gm = transconductance of the MOSFET

Input and Output Impedance Calculation

A good amplifier should have high input impedance and low output impedance.

Input Resistance is the resistance seen from the input terminals of the amplifier.

Resistance between G and S of the MOSFET is infinity(Gate current = 0)

Therefore Input resistance = R1|| R2

Zin = R1|| R2 = 1000k||1000K = 500K

Output resistance is calculated by calculating the resistance seen from the output terminal, when all the voltage sources are open circuited and current sources are short circuited. So the equivalent circuit will reduce to Fig: 4

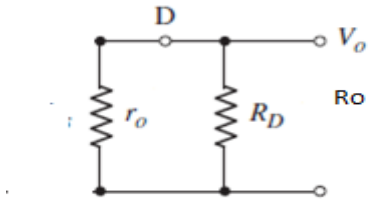

Figure 5 Output Resistance calculation

Zout = ro||R_D [3]

$ro = 1/(\lambda I_D)$

λ = 0.5

I_D = 0.1mA

ro = 20K

Zout = ro||R_D

= 20k||25k = 11.1K

Simulation

PSPCE EDA tool from Cadence was used to simulate the circuit.

Input Frequency = 10KHZ

Input Peak voltage =0.5V

Output Voltage =1.4V

Gain = 1.4/0.5 = 2.8

Fig: 2 shows the simulated waveforms of input and output.

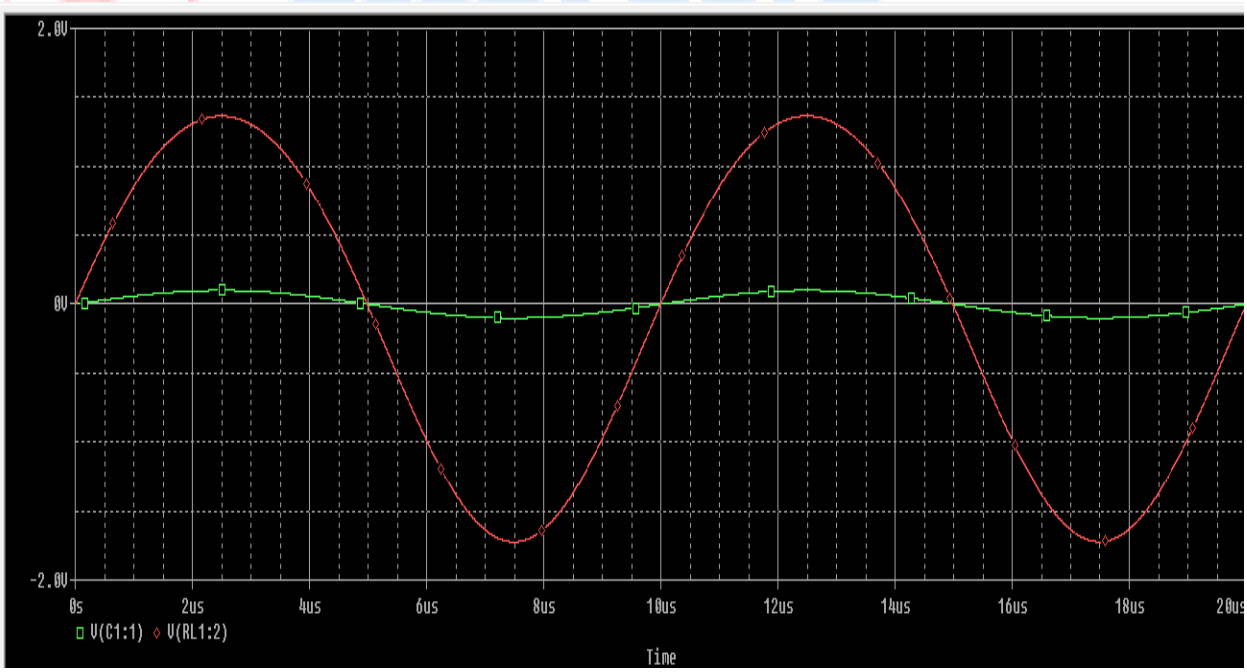

Figure 6 Simulation Waveforms of input and output

Fig: 3 shows the simulated single stage with all the DC conditions

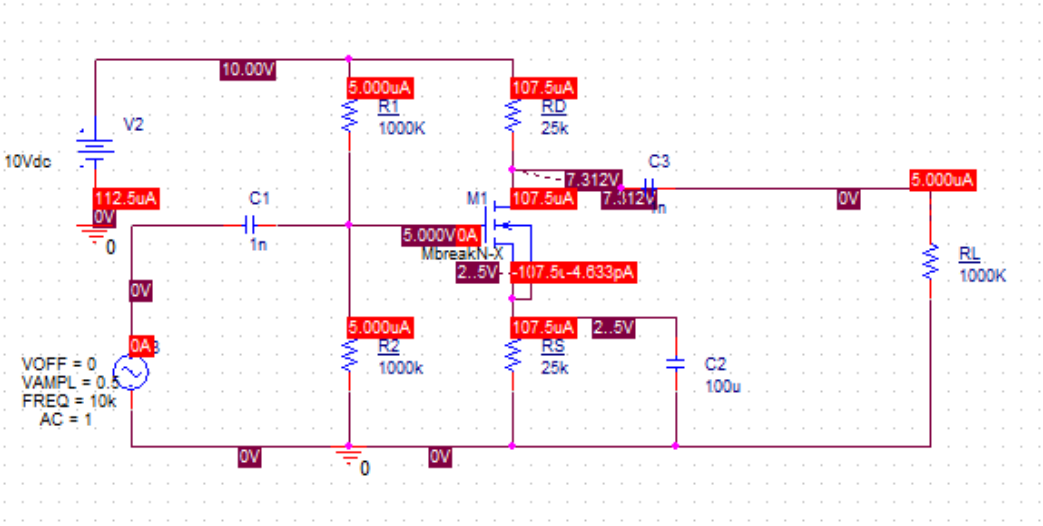

Figure 7. DC analysis simulation

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[3] http://www.ittc.ku.edu/~jstiles/312/handouts/Drain%20Output%20Resistance.pdf

[4] Electronic Devices and Circuits, David A Bell, Oxford University Press, 25-Jun-2009

[5] whites.sdsmt.edu/classes/ee320/notes/320Lecture31.pd

[6] http://www-inst.eecs.berkeley.edu/~ee105/fa14/lectures/Lecture13-Small%20Signal%20Model-MOSFET.pdf