For Assignment Help

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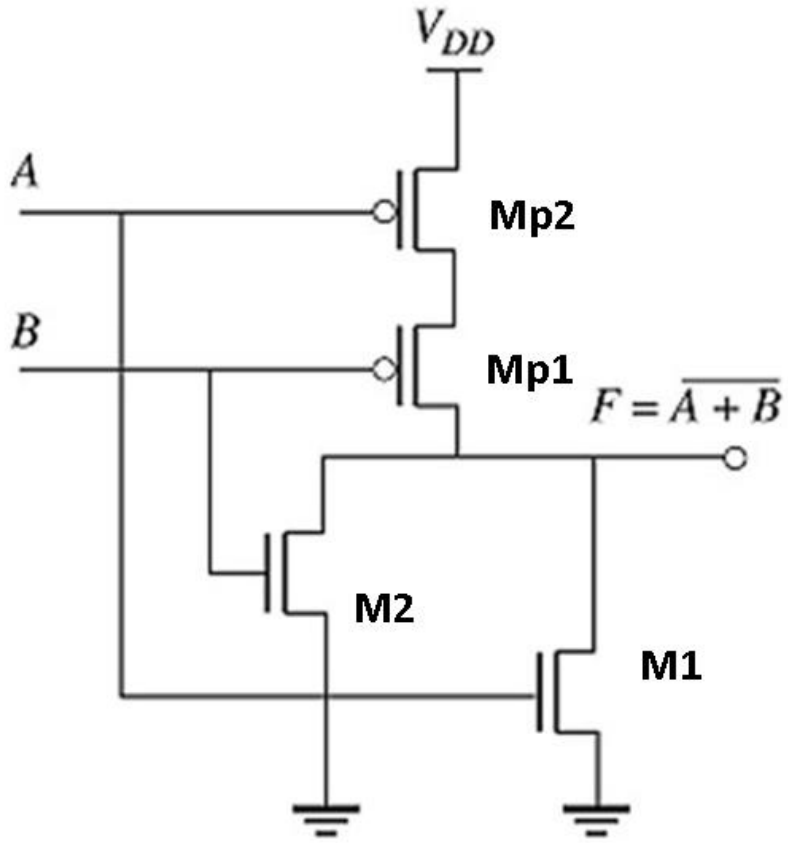
CMOS Design Assignment (2016)

Introduction:

- Designing a simple CMOS circuit consisting of two-input NOR gate.

Schematic of 2-input NOR gate:



- The schematic shows that there are 2 P-MOS Transistors (Pull up Network) in Parallel and 2 N-MOS Transistors in Series (Pull down Network).
- When A or B is high inputs, M1 or M2 will be ohmic and the output F will discharge to zero.
- When both A and B are low inputs, Mp1 or Mp2 will be the output F will charge to Vdd.

Calculations:

- **To calculate W/L)p and W/L)n**

  Lmin=0.2 um, (minimum Feature size)

  $\frac{W}{L})_p = \frac{\mu n}{\mu p} * \frac{W}{L})_n$, $\frac{\mu n}{\mu p} = \frac{.1}{.05} = 2$,

  but for optimum delay→ $\frac{W}{L})_p = 2.5\frac{W}{L})_n$

- Transistor sizing is chosen in order to minimize propagation delay as minimum as possible.

  Propagation delay: $tp_{hl} = \frac{Cl}{Kn\,Vdd} = 0.69 * Ron * Cl$

  To Calculate Ron, Start from current equation:

$$I_d = k\left[(V_{GS} - V_{th})V_{DS} - \frac{{V_{DS}}^2}{2}\right]$$

  And for very small V_{DS} we can neglect this term $\frac{{V_{DS}}^2}{2}$

$$\therefore I_d = k(V_{GS} - V_{th})V_{DS}$$

  Transistor acts as a resistor Ron

$$Ron = \frac{V_{DS}}{I_d} = \frac{1}{K(V_{GS} - V_{th})}$$

$$\therefore tp_{hl} = 0.52 * \frac{Cl*Vdd}{\left(\frac{W}{Ln}\right)Kn\,Vdsatn\left(Vdd - Vtn - \frac{Vdsatn}{2}\right)}$$, Kn= $\mu n * Cox * \frac{W}{L}$

  Threshold Voltage for N-MOS: Vtn=0.3v, Supply Voltage: Vdd=4v,

  Minimum Feature size: Lmin=0.2 um,

  Saturation Voltage: Vdsat=4-0.2=3.8v

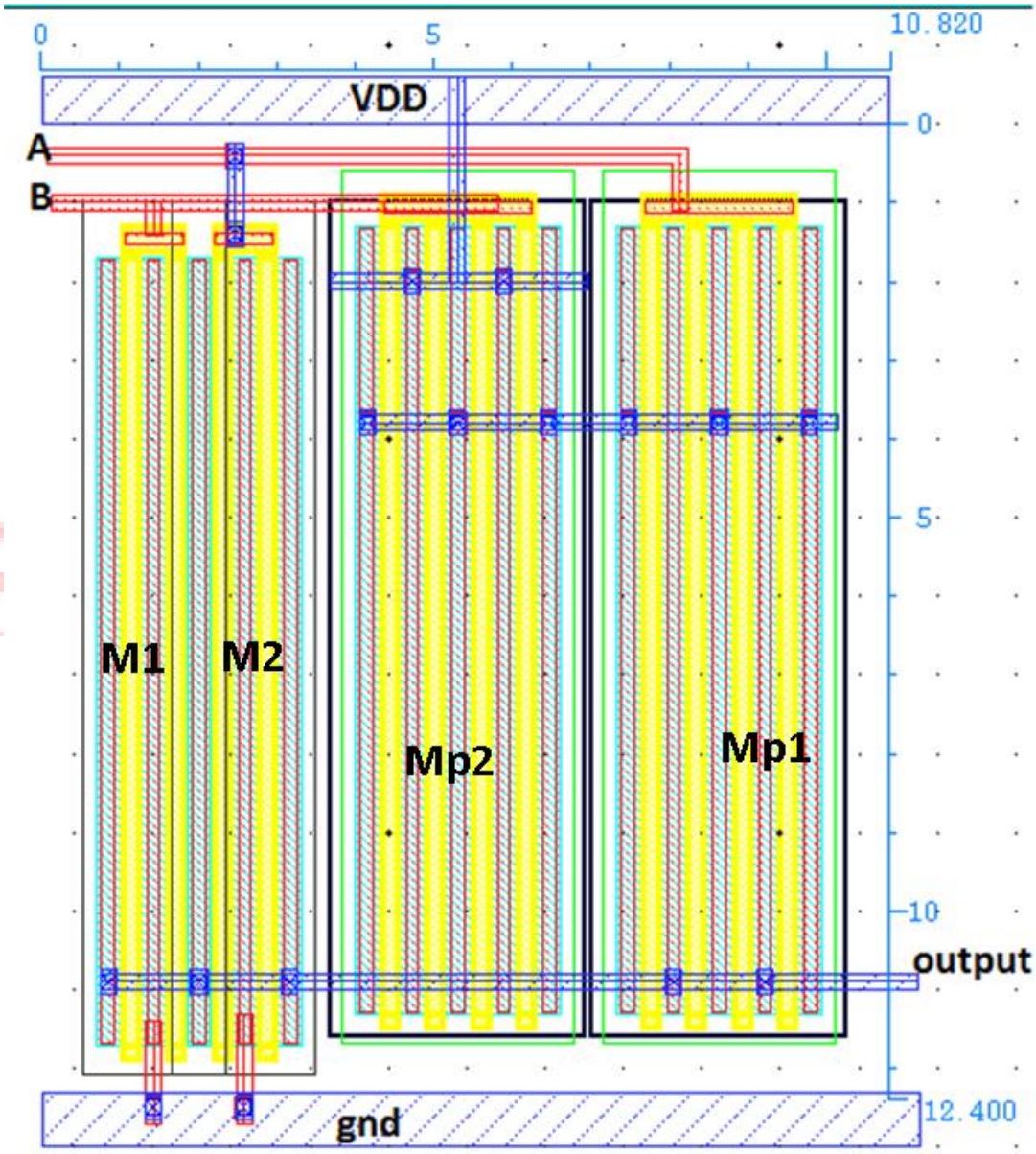
  For tp_{hl}=3.5*10^{-11}, Cl=Co=0.5nf → Wn=21,Wp=53

  Width for N-MOS= 21um

  Width for P-MOS= 53um

Layout:

1- Maximum alignment error=0.1 um → min routing width >0.1um.
   By using min routing width=0.2um.
2- Area should be minimized.



Metal 1	Metal 2	Poly	Diffusion	N-Well

Explanation:

- Using Cadence Virtuoso to draw the layout and verify the design rules and the simulations results for 2-input NOR gate.
- Following these steps to draw the layout:
    - **Drawing Transistors**
      To make p and n transistors. For p transistor using n-well and the background in the main layout window will act as your p-substrate. Thus the n transistors is placed directly in the p substrate. However the p transistor will be placed in n-well.
      Masks used for P transistor: N-well, diffusion, any poly.
      Masks used for N transistor: P-substrate, diffusion, any poly.

    - **Making Connection**
      The next step is to connect the drains of the two N transistors and the first P transistor together to make up the output. The source of the first P transistor is connected to the drain of the second P transistor which is source is connected to Vdd and the source of the two N transistors are connected to Gnd. The two gates of each (N and P) transistor are connected together to form one of the inputs.
      Metal 1: used for input A, and B.
      Metal 2: used for output, Vdd, and Gnd.

- **Drawn layers (Masks) used to create a transistor:**

  1) Well: NMOS are in P-well, PMOS are in N-well

  2) Diffusion: defines active vs. isolation regions on layout, and sets Source and Drain for transistor.

  3) Poly: gate mask over diffusion mask defines W and L of each transistor.

  4) Contact: defines the contacts between the masks.

  5) Tap: defines contact to substrate or well.

- **List of Rules to be Considered:**

  1) One layer: width, spacing

  2) layer to layer: spacing, enclosure, extension, overlap

  3) Rules are going to be separated into the masks: N-well, Diffusion, Poly, Contact, and Metal

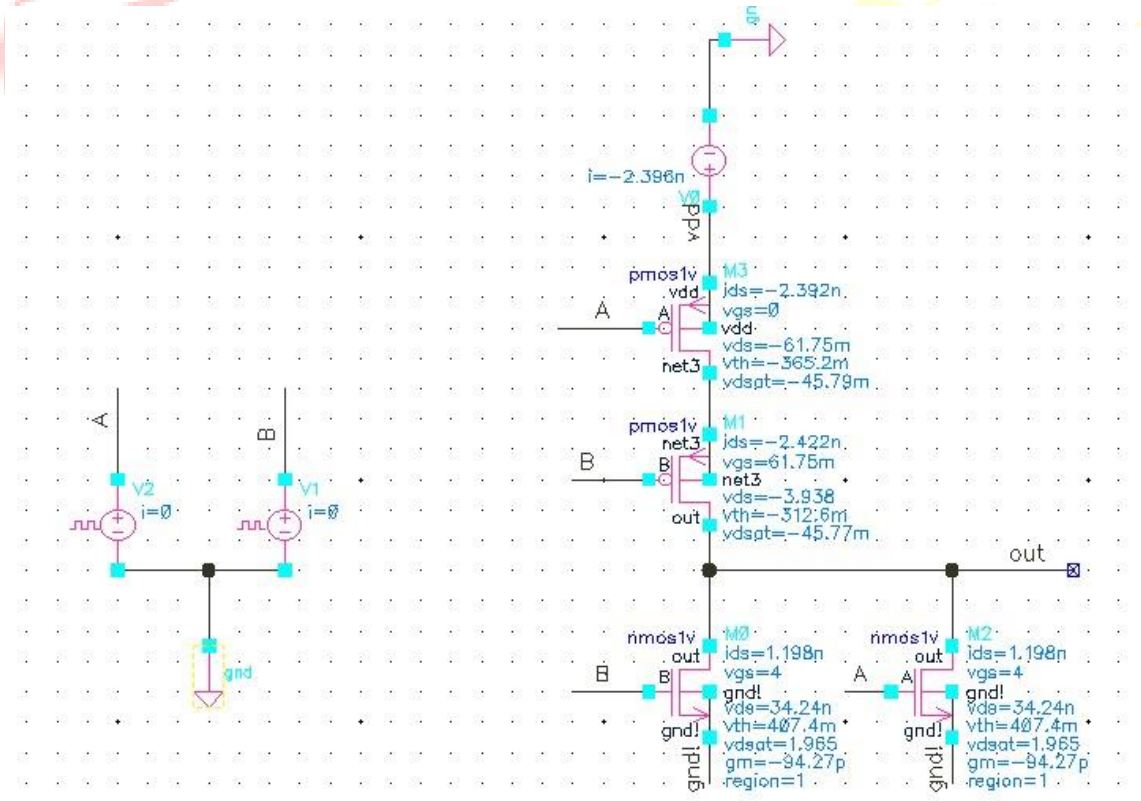
- **Explanation of Layout:**

  1) Layout PMOS and NMOS Transistors using calculated $\frac{W}{L})_{p,} \frac{W}{L})_{n}$ using Diffusion, Poly and Well Masks.

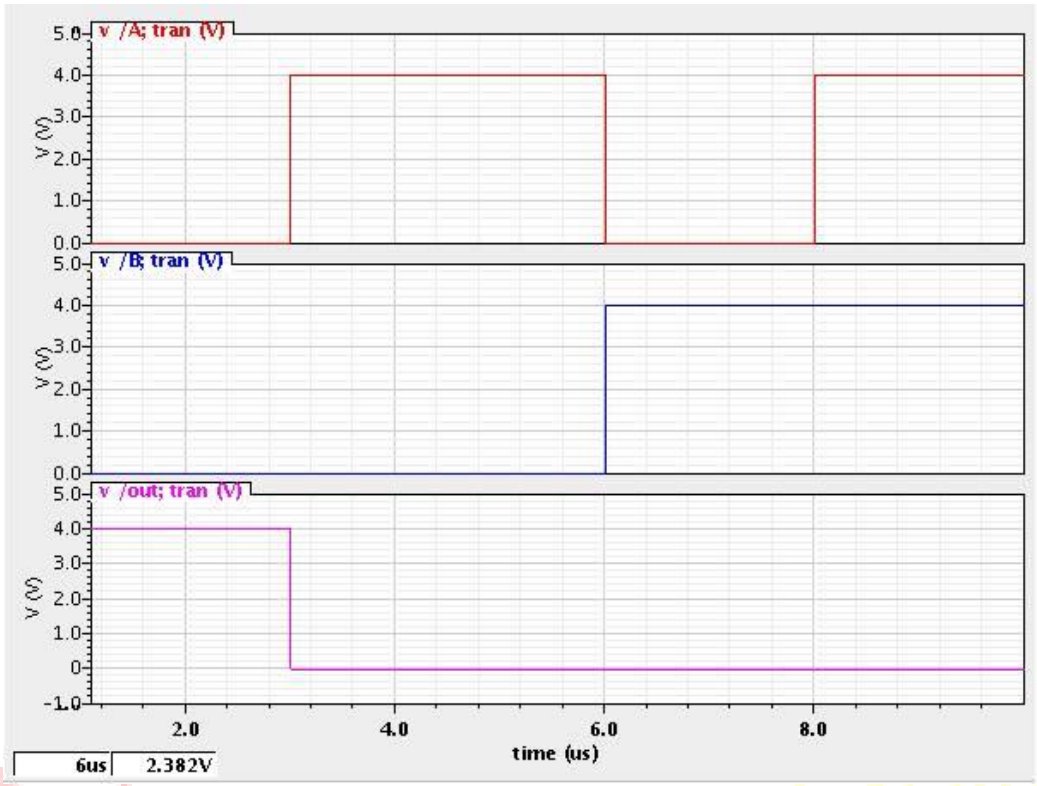
  2) make input and output ports using metal masks.

  3) Connect the masks using Contacts.

  4) label the ports and the power lines (VDD and GND).



Schematic from Cadence



Waveform Simulations from Cadence

A	B	F
0	0	1
0	1	0
1	0	0
1	1	0

Truth Table for 2-input Nor gate